IN THE CLAIMS:

No claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Previously presented) A method of fabricating an interposer substrate for attaching to an active surface of a semiconductor die having a plurality of conductive bumps protruding transversely therefrom, the method comprising:

providing a substrate having a first surface and a second surface, the substrate including a dielectric layer and a plurality of conductive elements on the dielectric layer adjacent the second surface;

forming a plurality of recesses in the first surface of the substrate and through the dielectric layer to a depth through the dielectric layer, each of the plurality of recesses exposing at least a portion of a contiguous conductive element adjacent the second surface and of a size and configuration to receive the plurality of conductive bumps of the semiconductor die so that the plurality of conductive bumps is substantially received within the plurality of recesses; and

forming at least one opening in the second surface of the substrate in communication with at least one recess of the plurality of recesses.

2. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises forming the plurality of recesses to a depth so that a surface of each of the plurality of conductive bumps will contact the at least a portion of the contiguous conductive element with the active surface of the semiconductor die abutting the first surface of the substrate.

3. (Canceled).

4. (Previously presented) The method of claim 1, wherein providing the substrate comprises forming the plurality of conductive elements by at least one of printing conductive ink and etching a conductive layer.

5. (Previously presented) The method of claim 1, wherein providing the substrate comprises disposing a solder mask over the plurality of conductive elements in a pattern leaving portions of the plurality of conductive elements exposed.

6. (Previously presented) The method of claim 1, wherein providing the substrate comprises providing the dielectric layer as a flexible polymer material.

7. (Previously presented) The method of claim 1, wherein providing the substrate comprises providing the substrate to include at least one of BT, FR4 laminate, FR5 laminate and UPILEX®.

8. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises collectively configuring the plurality of recesses in a centrally aligned row in the substrate to correspond with a conductive bump configuration on the semiconductor die.

9. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises collectively configuring the plurality of recesses in a peripheral configuration in the substrate to correspond with a conductive bump configuration on the semiconductor die.

10. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises collectively configuring the plurality of recesses in an I-shaped configuration in the substrate to correspond with a bump configuration on the semiconductor die.

11. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises forming the plurality of recesses by at least one of a wet etch, dry etch, mechanical drilling, mechanical punching and laser ablation.

12. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises patterning the plurality of recesses, each substantially with a peripheral shape including at least one of a square, rectangle, circle and oval.

13. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises forming at least one sloped side wall in each of the plurality of recesses.

14. (Previously presented) The method of claim 1, wherein forming the plurality of recesses comprises forming at least one side wall in each of the plurality of recesses to be substantially perpendicular with respect to the first surface of the substrate.